Low-Power and Low-Cost Dedicated Bit-Serial Hardware Neural Networks for Epileptic Seizure Prediction

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Abstract— **This paper investigates the feasibility of using bit-serial architecture as a method of designing an extremely low-power and low-cost neural network processor for epilepsy seizure prediction. The concept of a novel bit-serial data processing unit (DPU) is presented which implements the functionality of a complete neuron and uses bit-serial arithmetic. An array of these DPUs are controlled by a simple finite state machine. We show that epilepsy detection through such low-cost and low-energy dedicated neural hardware is feasible. The proposed processor extracts epileptic seizure characteristics from electroencephalogram (EEG) waveforms. In order to facilitate the classification of EEG waveforms we develop a dedicated feature extraction hardware that provides inputs to the neural network. This approach has been tested using various network configurations and has been compared with related work. A sample complete system which can predict epileptic seizures with high accuracy has been implemented on an ALTERA Cyclone V FPGA and the hardware uses 3088 ALMs which constitutes about 5% of the Cyclone V A7 capacity.**

I. Introduction

In recent years, the World Health Organization (WHO) have found that 50 million of the world's population are affected by a hidden disability known as epilepsy [1]. Approximately 80% of the reported epileptic cases occur in developing countries where readily available treatment facilities and medications are not generally accessible. Currently, epilepsy is commonly treated with the use of anti-epileptic drugs (AEDs). Early and accurate seizure prediction is essential in preventing seizures by the timely administration of such drugs. Existing state-of-the art seizure prediction systems rely on complex software methods and require significant CPU power. These methods use elaborate mathematical models of non-linear dynamic systems which are solved using time-domain or frequency-domain analysis [2]. Artificial Neural Networks (ANNs) have also been shown to predict epileptic seizures reliably with an accuracy over 90% [3]. ANNs are an efficient classifier used commonly in conjunction with linear numerical methods of feature extraction to facilitate epilepsy detection. However, as of today, there is still no reliable, home-based and low-cost seizure prediction system which could be used as an aid for timely administration of AEDs and used by an individual epileptic patient. In this paper we propose to consider simple, dedicated hardware neural networks that are optimised for seizure prediction from electroencephalogram (EEG) waveforms and can be personalised to reflect the characteristics of an individual patient. Such systems can be implemented in the form of affordable, wearable equipment without the need to resort to complex software and powerful computers. Firstly, we briefly review state-of-the-art seizure detection methods. We focus on linear seizure prediction models [4] which have the advantage of simplicity and versatility compared with non-linear ones that are capable of addressing the non-stationary nature of the EEG signals. Secondly we present a dedicated hardware implementation of an artificial neuron, based on a bit-serial Data Processing Unit (DPU) which is extremely small and can be used in vector arrangements where a single sequential controller drives an array of such DPUs. We demonstrate that the proposed DPU has has the capability of simulating a biological neuron and can be expanded into a neural network that successfully differentiates between epileptic seizure and non-seizure EEG waveforms. The EEG waveforms used in our investigation are taken from real patients and available online [5] in public domain.

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II. Conventional Classification Methods for Epilepsy Detection

Here we summarise briefly the main conventional classification techniques for machine learning which are applicable to medical diagnosis including epilepsy. These methods are the Naive Bayes Classifier, Decision Tree Classifier, k-Nearest-Neighbours (k-NNs) Classifier, support vector machines (SVM) and classifiers based on neural networks. They are briefly reviewed in the following subsections.

A. Naive Bayes (NB) Classifier

NB is a simple probabilistic classifier utilising the Bayes Theorem. It can also be considered as a conditional probability model. This classifier is often used in data mining and it is also applicable to automated medical diagnosis thus making it suitable for epilepsy detection. The Naive Bayes classifier uses the independence assumption that focuses on each feature independently of each other while ignoring any possible correlation between the features [6]. One of the main advantages of using the Naive Bayes classifier is the limited use of training data for classification.

B. Decision Tree Classifier (DTC)

Decision trees are an efficient way to classify sets of data. As a sample is only tested against a subset of the classes, traversing a decision tree does not require complex computations. It has been suggested recently [7] to use neural networks are used in the design of a DTC. There are a few disadvantages when using a decision tree. It will not be as accurate as the other classifiers. Furthermore, the performance of the DTC will heavily depend on the effectiveness of the particular design [7]. DTCs tend to be less robust than other methods as a very small change in the training datasets might result in a huge change in the output prediction.

C. k-Nearest-Neighbours (k-NN) Classifier

A k-NN classifier is a non-parametric, non-linear yet relatively simple classifier. This classifier is effective when dealing with large data sets. It relies on class assignment based on a nearby data set where similarities between the samples used are measured with a distance function. A recent work [8] points out that k-NN is applicable to medical classification problems. The basic algorithm for a k-NN classifier is relatively similar to that of a neural network classifier. Both have a training stage and a prediction stage. The training stage of the k-NN classifier involves all the different samples which are stored in a form of memory. A neural network, on the other hand, uses the training stage to calculate the weights with the highest accuracy to predict a target output.

D. Support Vector Machine (SVM) Contribution to Epilepsy Detection

SVMs have been used to analyse EEG signals which contain a great deal of detail about the brain activity. A smart sensor IC was proposed [9] with a CMOS chip that has an area of $0.35um$ for scalp EEG acquisition. This chip is integrated with the local processing of the sensor node. Feature vectors of the signal are extracted and classified through machine learning. In order to produce a functional system for epilepsy detection, a number of sensors would have to be worn to achieve spatial correlation. Each individual output of the classifier could then be combined to detect the onset of an epileptic seizure.

Support Vector Machines have also been used in lung cancer diagnosis in conjunction with image processing techniques [10]. SVMs are suitable for such applications as they possesses the advantage of high generalisation and an assurance of global optimisation. They have been successfully used in many other fields that require classification.

E. Automatic Epilepsy Detection Using Artificial Neural Networks (ANNs)

It is possible that the prediction of the onset of a seizure occurrence can be achieved with the assumption that the EEG generated is a very complex but linear system. However, the brain is non-linear. By analysing the power spectrum, it is also possible to continue the analysis through a linear approach [11]. Back propagation neural networks include two stages, a forward propagation stage and a back propagation stage. The normal neural operation uses the forward propagation to pass along the EEG sample provided along the input layer to the hidden layer where calculations are being made which in turn is passed to the output layer to produce the output sample of the neural network which can determine if a seizure occurrence will appear with the input EEG sample. The back propagation stage includes a learning process which reduces the error between the calculated output sample and the target output (possibility of seizure occurrence). This process is performed by adjusting the weights of the neural network in real time [11]. Spiking Neural Networks (SNNs) are a third generation ANNs that have been researched in recent years [12]. SNNs are different from other forms of ANNs as each individual spiking neuron propagates information by the timing of the neuron, rather than using the rate of the spikes. It was also found that SNNs are effective in brain modeling [13], [14]. This is useful as methods can be sought to detect epilepsy through the process of modelling the brain of an epileptic patient. Hardware implementations of SNNs were performed using NVIDIA CUDA [12]and the SpiNNaker [15]. The latter has the capability to simulate and implement the SNN which is used in brain modelling mentioned above. There are a few advantages and disadvantages when using hardware implementation on NVIDIA GPUs. The constant read-only memory is proved to have higher access speed than global memory. However, there is a requirement for more graphics processing unit (GPU) memory. Accessing the parameters of an individual neuron is also slow [12].

III. Bit-Serial Architecture with Relation to Neural Network Processors

Bit-serial architectures which process data bit by bit during each clock cycle are largely historic. Most modern processors use bit-parallel data processing for performance. However, when high performance is not a priority but instead the emphasis is on very low-power and low-cost bit-serial computing has its advantages. In modern applications bit-serial processing is still used sometimes in digital filters where input samples are processed in a bit-serial manner, although. Usually, however, the overall samples included in the filter's window frame are processed in parallel.

IV. A bit-serial hardware neural network

A novel approach is proposed to implement a low-cost hardware neural network which is primarily intended for use in portable equipment to predict epilepsy seizures. We consider the classical model of a perceptron that receives a vector input pattern x_i where $i = 1, \ldots, I$ and I the size of the vector. These inputs are weighted by the weight vector of a given perceptron $(w_1, w_2, \ldots, I)$ which is obtained in the off-line learning process. The neuron is a summation unit that performs the sum of products to calculate its output u. The output u is then processed by the activation function used in the output neuron. In our case the activation function is a simple threshold operation converting u into a logic signal y which has the value of '0' or '1'.

$$u = \sum_{i=1}^{I} w_i x_i \tag{1a}$$

$$y = \Phi(u) \tag{1b}$$

The conventional bit-serial architecture can model this behaviour with ease and complex feed forward neural networks (FNNs) based on such neurons can be created using simple, regular hardware structures controlled by simple state machines. The learning process of such designs can be accomplished off-line by using simulation software.

Each DPU in a given FNN layer performs the same operations and receives control signals issued by the layer control FSM to carry out the bit-serial additions and multiplications. This way, an FNN layer becomes an SIMD machine controlled by a single FSM. The development of an FPGA implementation of the neural processor is fast straightforward. We have used an FPGA implementation to carry out a number of test and study the potential of the proposed processor to classify epileptic EEG patterns. Table I shows that an 8-bit DPU requires only 24 Logic Elements (LEs) on an inexpensive Altera Cyclone V FPGA, out of over 300,000 LEs available on a Cyclone V chip. The control path of for a network with three layers requires 103 LEs (Central Control FSM: 3 LEs, 2 layer FSMs: 18 LEs each and 2 counters: 32 LEs each). This compares favourably with the size of the datapaths of typical bit-serial processors mentioned in the Table. Bearing in mind that the control logic of the proposed approach requires only simple state machines, rather than fully-fledged program control paths used in general-purpose processors, expected overall benefits of an ASIC implementation will include faster operation and lower power consumption.

Hardware	**Development Chip**	**LE Count**
Bit Array [16] Processor	ASIC	56 Altera Equivalent LEs
Cellular Processor [17] (Data Path)	Virtex 5	26 Altera equivalent LEs
Proposed Neural Processor	Cyclone V	24 LEs

TABLE I: Cost comparison between three different processors from previous work [18].

V. Proposed Feature Extraction Hardware - Slope Calculator

In order to complete the wearable seizure detection system, it is imperative to include a novel and simple feature extraction hardware to provide the inputs to the BSNN. The proposed hardware will use picoMips as the basis of the design.

The data path consists of two synchronous RAM and a simple subtractor in the form of a ALU module. The data path is controlled by a simple FSM module. The hardware cost requires only 13 ALMs when synthesised on a Altera Cyclone V chip. This hardware will serve as a mean of extracting slope of the EEG waveform from two adjacent points on the sample.

VI. EEG Waveform Classification

The input data used in the evaluation of the proposed FNN was obtained from an on-line open source [5] which provides sets of EEG waveforms for both seizure free instances and EEG waveforms during seizures taken from the brain (epileptogenic zone) of the same patient. Figure 2 shows an samples of an epileptic and a normal EEG. Our results we obtained from a number of implementations of the proposed FNN and were evaluated using standard metrics [19] in seizure detection, namely: the sensitivity (TPR), specificity (TNR), positive predictive value (PPV) and negative predictive value (NPV). The hardware implementations were trained offline in MATLAB and then tested with two sets of 100 EEG waveforms. As part of the validation process, the same input data used for training was used to test the n-1-1 network (i.e. n neurons in the input layer, one neuron in the hidden layer and one output neuron).

It was found that the n-1-1 network configuration exhibits very bad recognition rates. From the results it can be concluded that a multi-input single neuron in the hidden layer is not sufficient to detect epilepsy accurately. Therefore, other configurations have been tested, for example a 40-n-1 network with n hidden neurons. The DPUs used in these tests had a 12-bit precision to provide high accuracy. In summary, the network configuration 40-30-1 provides promising results in terms of detecting epileptic waveforms. Further tests have been conducted using a larger number of inputs and more hidden layers to further validate and optimise the network.

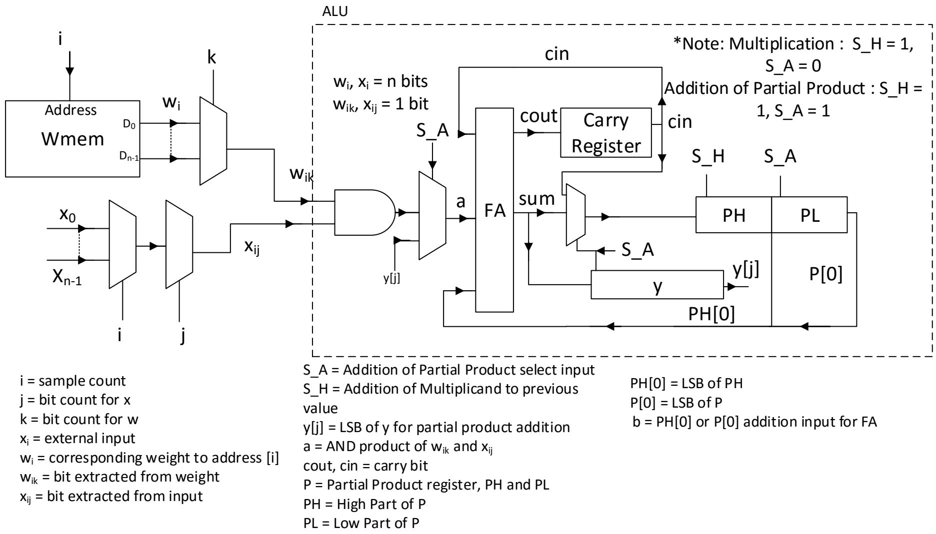
A. Hardware Network Validation and Testing

As the main purpose of this work is to distinguish seizure-free waveforms in epileptic patients from seizure waveforms, healthy patient brain waveforms are not included in the design testing. Results of the tests carried out at the validation stage have been compared with those of various software methods used in epilepsy detection [3].

Using the training datasets, the 11-7-1 hardware neural network with a 12 bit architecture has a specificity and sensitivity of 60%. It could recognise 30 out of 50 waveform used to train the network in a MATLAB model. The feature vector values consist of the same metrics as those provided in related work [3]. These values contain mean (X_{Mean}), median (X_{Median}), mode (X_{Mode}), standard deviation (X_{StdDev}), first quartile (X_{Q1}), third quartile (X_{Q3}), inter-quartile range (X_{IQR}), skewness (X_{skew}), kurtosis ($X_{kurtosis}$), minimum (X_{Min}), and maximum (X_{Max}). Ten other network configuration have been designed and tested. These configurations analysed using MATLAB in order to determine the mean square error (mse) in each case. From Table II, it can be seen that a single hidden layer with 100 neurons has a similar performance to that of a double layer network with 10 neurons in each layer.

B. EEG Waveform Slope Used as Feature Vector

In the previous subsection, a feature vector consisting of various statistic metrics is used. The maximum accuracy was 80% when tested using additional data. However, disparities



bit	LE Cost	
	Cyclone V	Stratix IV
6	20	20
8	24	28
12	28	33

Fig. 1: DPU Design with logic element counts included in table.

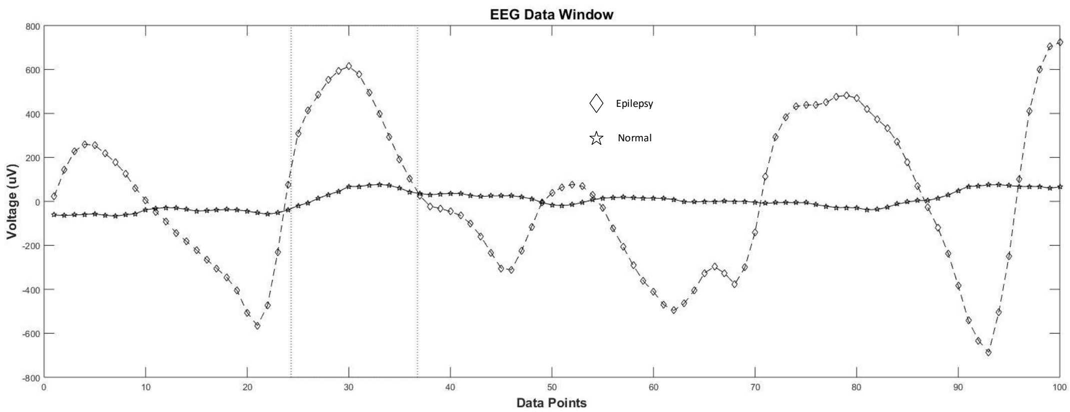


Fig. 2: Sample EEG input data.

Network Configuration	Correct recognition against training data	Correct recognition against additional tests
11-25-1	52%	60%
11-40-1	56%	50%
11-65-1	60%	30%
11-100-1	66%	55%
11-10-10-1	62%	60%
11-20-20-1	56%	80%
11-30-30-1	58%	60&
11-40-40-1	64%	45%
11-10-10-10-1	54%	50%
11-5-5-5-1	56%	30%

TABLE II: Correct recognition rates of different hardware ANN configurations.

when testing the same network configuration against the training data should be noted. In this respect, the 11-20-20-1 network shows some promising results. In this section, some experiments have been conducted to obtain better accuracy by using the slope of the EEG waveform at different points as a feature vector. The tested network configurations are 11-10-10-1, 11-20-20-1, 11-30-30-1 and 11-40-40-1.

Network configuration	TPR	TNR	PPV
11-10-10-1	57%	100%	80%
11-20-20-1	52%	44%	42%
11-30-30-1	66%	64%	58%
11-40-40-1	63%	100%	100%

TABLE III: Statistics for network configuration evaluation against training data.

VII. Conclusion

In conclusion, experiments with bit-serial neurons confirm that an extremely small logic system can successfully implement effective epileptic seizure detection. The

Network Configuration	TPR	TNR	PPV
11-10-10-1	75%	33%	43%
11-20-20-1	50%	50%	40%
11-30-30-1	25%	44%	10%
11-40-40-1	53%	33%	80%

TABLE IV: Statistics for network configuration evaluation against additional data.

key benefit of a dedicated neural processor compared to known, equivalent general-purpose processors, is that very small control logic and a low bit-precision are sufficient to obtain correct operation. Multiple tests have been conducted with various network configuration to test the feasibility of detecting epilepsy when using the proposed approach. Future work involves further investigation into suitable sizes and accuracies of bit-serial FNNs which will be followed by a development of a low-power ASIC.

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